



SHEET 1 OF 1

INFORMATION DISCLOSURE
CITATION IN AN
APPLICATION

ATTY. DOCKET NO.
066365-0021

SERIAL NO.
10/813,433

APPLICANT
Simon KNOWLES

(PTO-1449)

FILING DATE
March 31, 2004

GROUP
2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
RF		US 5,423,051	06-06-1995	FULLER et al.	
		US 2005/0044434 A1	02-24-2005	KAHLE et al.	
		US 2003/0154358 A1	06-14-2003	SEONG et al.	
		US 5,600,810	02-04-1997	OHKAMI	
		US 6,725,357 B1	04-20-2004	COUSIN	
		US 6,880,150 B1	04-12-2005	TAKAYAMA et al.	
		US 5,956,518	09-21-1999	DEHON et al.	
		US 2002/0010852 A1	01-24-2002	ARNOLD et al.	
		US 2002/0174266 A1	11-21-2002	PALEM et al.	
		US 6,061,367	05-09-2000	SIEMERS	
		US 2002/0063577 A1	05-30-2002	ABBOTT	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code-Number + Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
RF		BOLOTSKI, et al., "Unifying FPGAs and SIMD Arrays," M.I.T. Transit Project, February 8, 1994, pp. 1-22, Transit Note #95.
		STOKES, "A Brief Look at the PowerPC 970," Ars Technica, 2002, pp. 1-3.
		BEEBE, et al., "Instruction sequencing control," IBM Technical Disclosure Bulletin, May 1972, pp. 3599-3611, Vol. 14, No. 12.
		SIMONEN, et al., "Variable-Length Instruction Compression for Area Minimization," IEEE, 2003.
		TANENBAUM, "Structured Computer Organization," 1984, pp. 10-12, Prentice-Hall, Inc., Englewood Cliffs, NJ.
		ALIPPI, et al., "Determining the Optimum Extended Instruction-Set Architecture for Application Specific Reconfigurable VLIW CPUs," IEEE, 2001, pp. 50-56.
		International Search Report issued in corresponding International Application No. PCT/GB2005/001073, dated April 5, 2006

EXAMINER
/Ryan Fiegler/

DATE CONSIDERED
12/11/2006

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 509. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.